ASIC Development for SNAP

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OVERVIEW

Context

Motivations for ASICS

Front-end partition and custom parts

R&D schedule

Status

Deliverables

Manpower and Costs

SCIENCE REQUIREMENTS

- **Minimize readout noise to allow stacking of multiple exposures**

  Total readout noise (CCD + RO) : 4 e at 100 kHz

  Amplification and signal processing : 1 e

  Channel to channel crosstalk less than 1/1000

- **Dynamic range**

  16 bits

- **Radiation tolerance:**

  3 years

ISSUES FOR ASICs R&D

Keep noise, linearity and power within the required limits,
before and after 20 kRad irradiation

Produce space qualified deliverables

CONTEXT

Sensors

Imager : 236 CCD's and 24 HgCdTe devices (FIDO)

Spectrograph : 2 CCD's and 2 HgCdTe devices

Temperature : CCD/HgCdTe array + cold electronics at 135-150 K

Readout electronics

Distance :1m

Temperature : -10 to 30 C

Power

Less than 500 mW per CCD/HgCdTe device for readout+digitization

Radiation

10 kRad total , 2 10^7 MeV/g NIEL

JUSTIFICATIONS FOR ASICs

Commonalities with High Energy Physics experiments:

Multichannel detectors

Environment under radiations

Power critical

BENEFITS

POWER

Integration into ASICS reduces the power needed to drive highly capacitive interconnect media

Power is reduced by at least one order of magnitude

RELIABILITY

Large dimensions interconnects such as connectors, solderings, bonding wires are less numerous for a given complexity

Mature radiation-hard IC processes allow the integration of reliable analog and digital components

VOLUME AND WEIGHT

The most obvious benefits

DRAWBACKS

DEVELOPMENT TIME

IC design is a lengthy process, the least error may induce several months delays

FLEXIBILITY

Once integrated, a component cannot be modified

ASICs versus DISCRETE

POWER

MegaCam	7.5 W/CCD (dicrete)
SNAP	0.5 W/CCD (ASICS)

RELIABILITY

MTBF	scales down as the number of soldered connections

VOLUME AND WEIGHT

CDS	1-4 ASICS / 12 discrete parts (8 Amp + 4 ADC drivers)
Clock driver	2 ASICS/ 10(or more) DACs + analog switches
	+ control FPGA's
	Lighter by a factor 5 at least + smaller size

Sample Front-End Electronics Partition

Analog processing (CDS)
Analog to Digital conversion on 16 bits
DC bias voltages generation
Clock signals generation
Interface to Data Acquisition System

ASIC 1

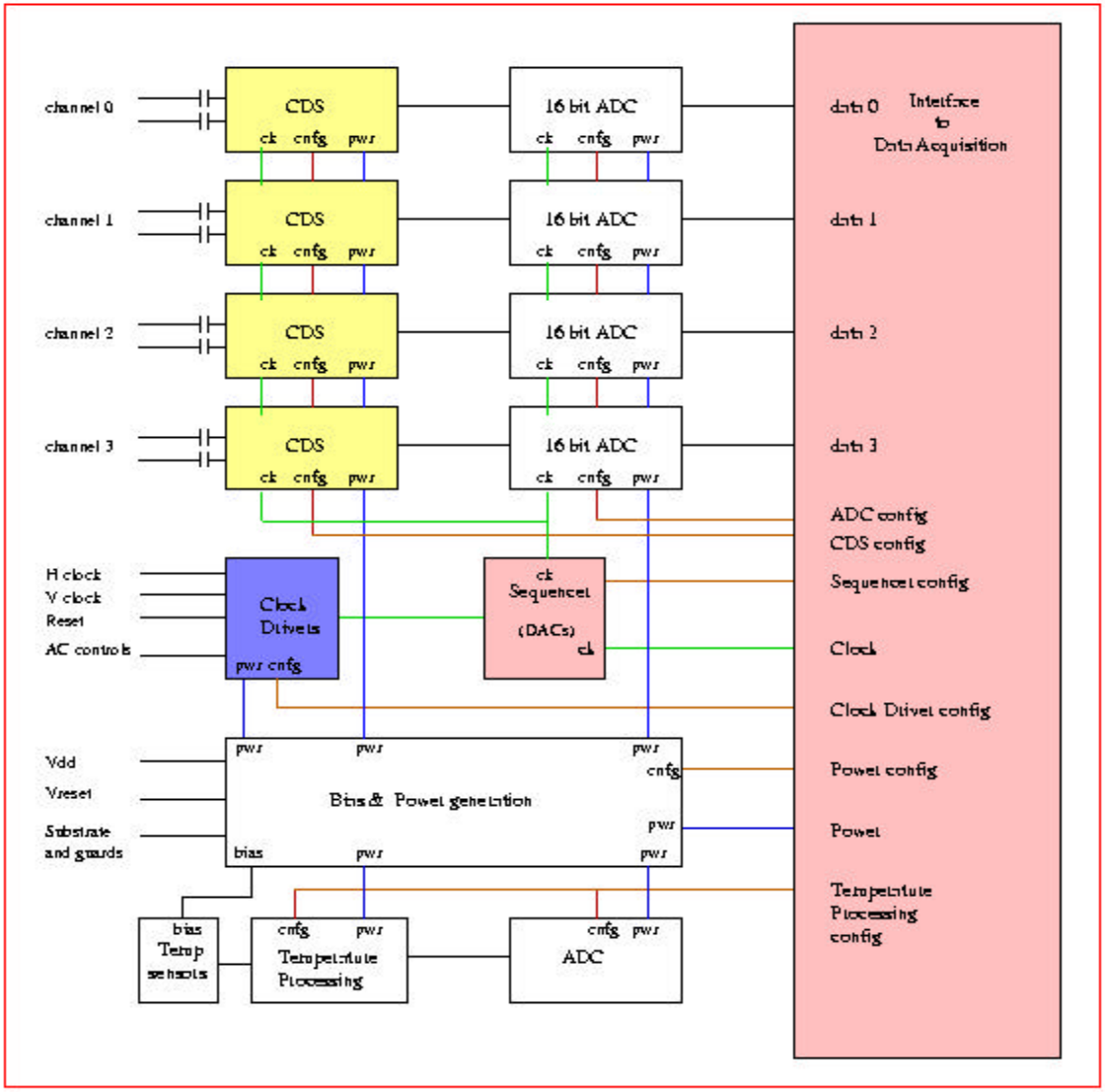
Correlated Double Sampler chip
Analog rad-hard (Bi)CMOS

ASIC 2

Clock Driver chip
Analog high-voltage rad-hard

ASIC or FPGA

Sequencer and interface
Digital rad-hard CMOS
or mixed rad-hard CMOS



STATUS

CDS CHIP

- Specified (document available)
- First prototype in radiation-hard technology submitted end-November 2000
  Return expected in April 2001
- Second technology under investigation

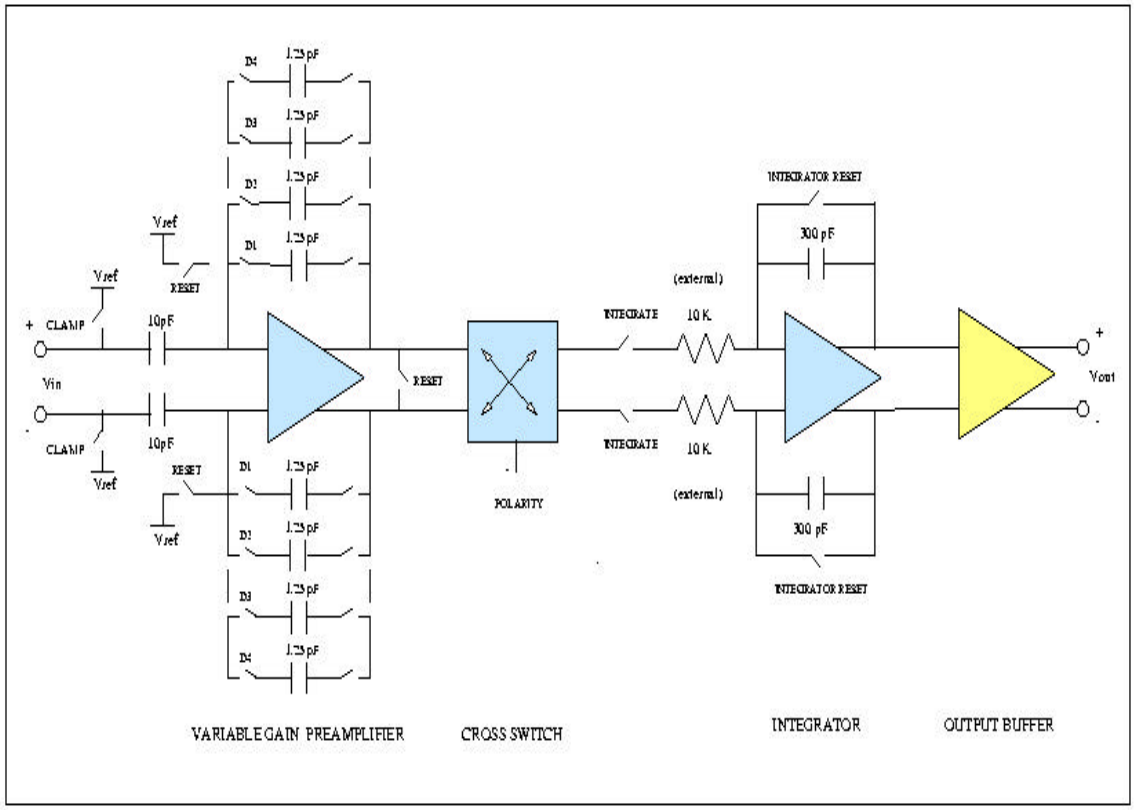
CLOCK DRIVER CHIP

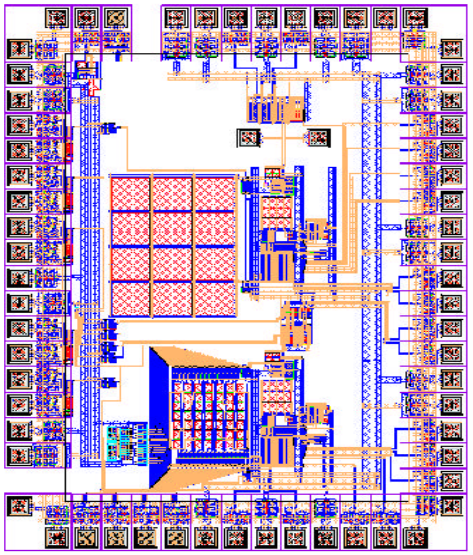
- To be fully specified
- Partition between :
  - Sequencer chip (digital)
  - Analog voltages generation (DACs)
  - Power buffers (-6V +6V voltages to CCD clocks)
- Technology under investigation
  - A sequencer chip has been designed by RAL (UK) in ATMEL (0.7 um CMOS) and DMILL technologies

CDS Chip Specifications

		Justification
CDS technique		
Double integration		Cancel the CCD kTC reset and 1/f noises
Integration gate:	4 to 8µ s	Filter the high frequency thermal noise
Input		Match the CCD sensitivity (6 µ V / e-)
Sensitivity:	0 - 1.56 V differential	
Noise :	1 CCD electron equivalent	Keep total readout noise close to CCD intrinsic performance
Output		
Gain selectable:	1-8 by steps of 0.5	Match the required CCD dynamic range (noise - full-well)
Output:	0 - 2.5 V differential	Match the ADC range
Linearity:	1/1000	Do not degrade the CCD linearity performance
Temperature	-10 - + 30 C	Temperature range of the readout electronics
Power	< 50 mW / channel	Keep total power below 75 Watts during readout

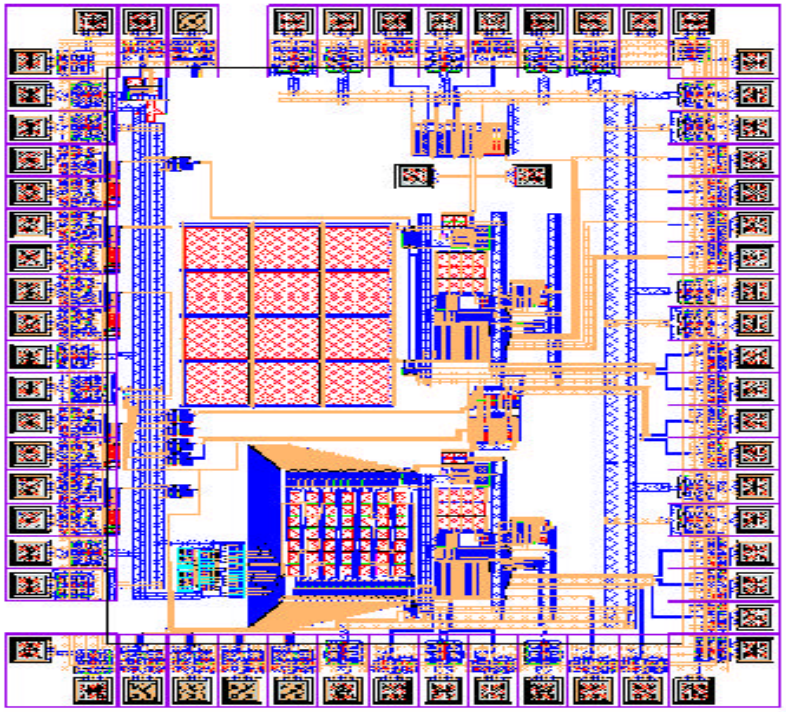
CDS Prototype Chip Block Diagram and Layout



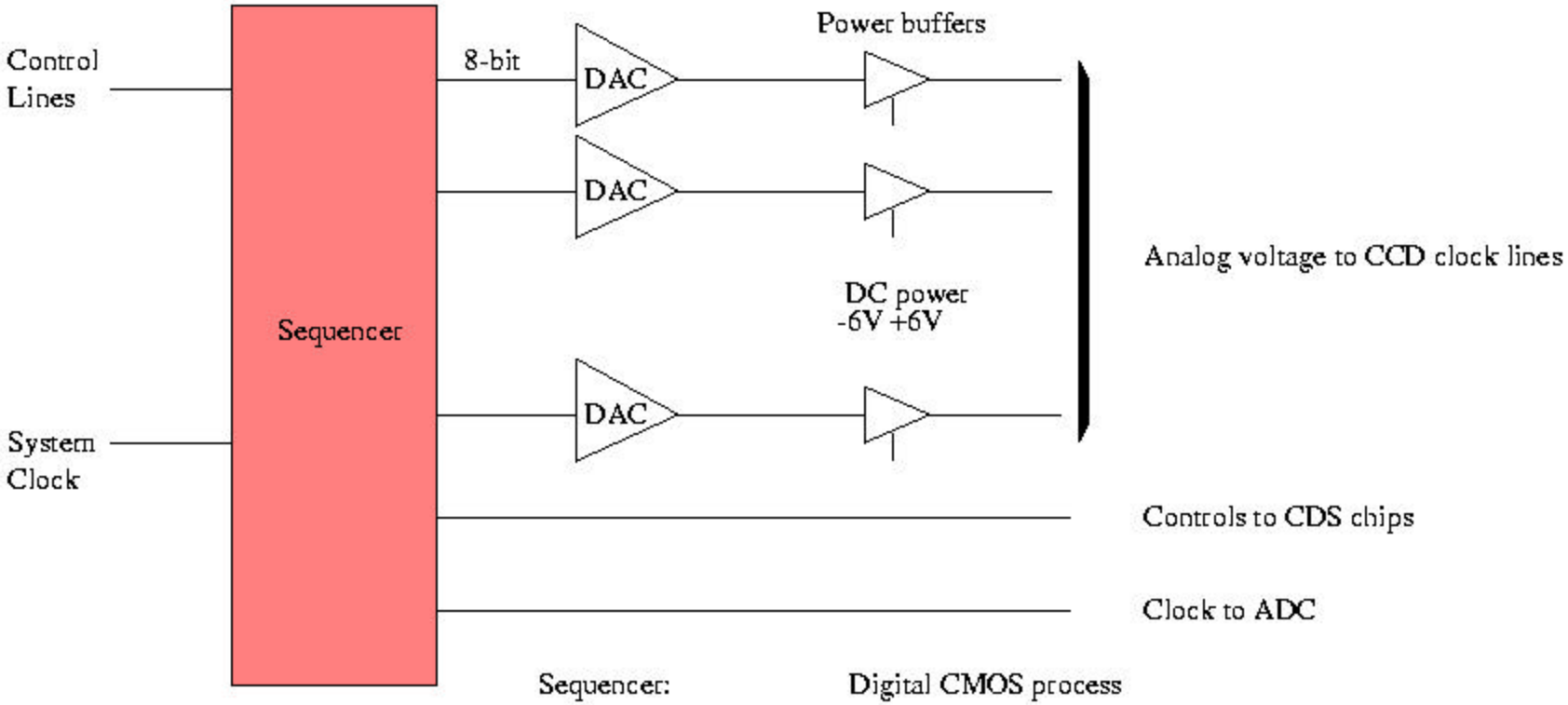


First prototype version

CDS Prototype Chip Layout (Nov 2000)



Sample Implementation of control chip



The sequencer may also integrate some interface to system functions

Other possible partition: Sequencer + DACs in analog-digital process, Power buffers in high voltage process.

Candidates IC Processes

	DMILL	Harris-Intersil UHF2	Harris-Intersil RSG	Peregrine	TSMC
Gate length (µM)	0.8	0.6		0.5	0.25
Voltage (V)	5.0	6.0	40.0	3.3	2.5
Radiation tolerance	10 Mrad	300 kRad	300 kRad	100 kRad	50 Mrad
Turn-around (weeks)	25	18	14	8-10	16
R&D costs ($/mm^2)	32	115	115	37	56
Production costs ($/mm^2)	44	36	60	27	58
# of submissions/year	4	tbd	tbd	3	12
ASIC	CDS/Sequ.	CDS/Sequ.	Clock Driver	CDS/Sequ	CDS/Sequ

SUMMARY

The ASIC R&D program was initiated in 2000

Main goals :

Meet the Science requirements

Improve noise performance/discrete

Improve the power budget/discrete

Improve volume and weight

Target date:

Equip a GigaCam demonstrator in June 2003